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Design and Implementation of a Chip Multiprocessor with an Efficient Multilevel Cache Based on Bus Arbitration Techniques

By

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Abstract

Computer designers utilize the recent huge advances in Very Large Scale Integration (VLSI) to place several processors on the same chip die to get Chip Multiprocessor (CMP). A CMP is the dominant architecture to improve the performance of the current computing systems. Several advantages are offered by CMP including, high performance, faster design, easier verification, and low power consumption comparing to a complex single processor. However, accessing a shared data by several processors is a primary challenge in the CMP. The data consistency must be reached among all memory hierarchies to ensure correct behavior and get higher performance. Moreover, optimal utilization with fair distribution of the shared resources such as the shared bus, represents another challenge. This thesis, proposes a CMP platform with multilevel cache, which is designed and implemented in order to improve the overall performance. A methodology in this work starts by designing a single pipelining MIPS processor. Then, a multilevel cache with a combination of write policies is offered to enhance some properties of data memory access such as miss rate and latency. After that, two bus arbitrations schemes are proposed to connect many processors on the same bus. Finally, the proposed CMP system with four processors and their multilevel cache has been implemented using Hardware Description Language (VHDL) on Altera's FPGA chip. The results show that the proposed multilevel cache with combination of write policies improves the miss latency by at least 10% comparing to other architectures. Also, the proposed bus arbitration schemes overcome the traditional bus arbitrations' shortcomings.